


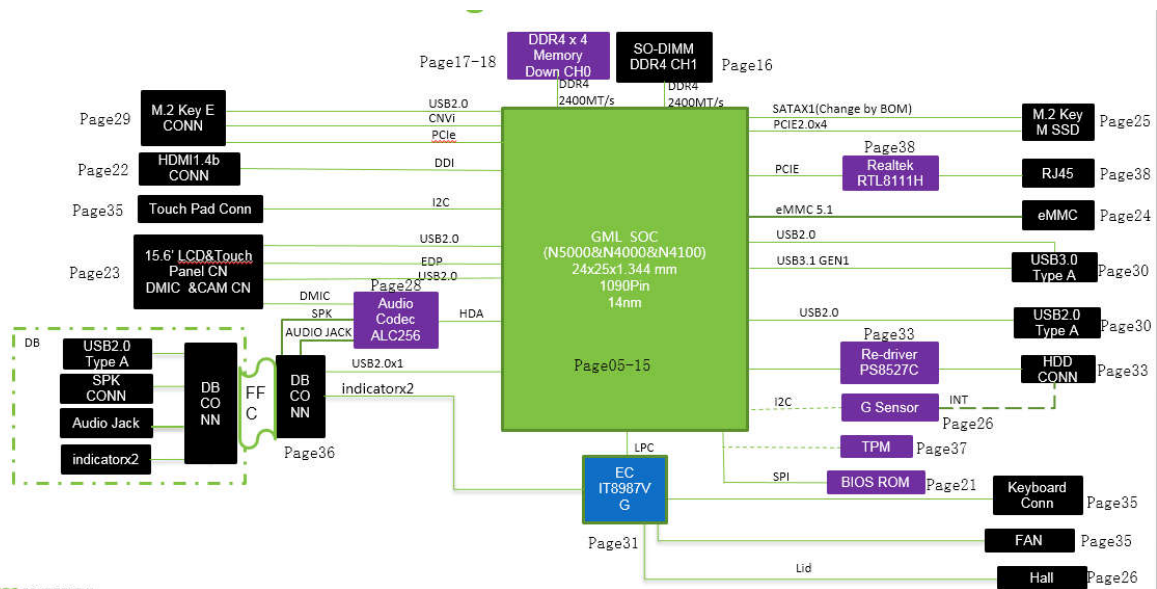
NB8609 V4.0 DDR4&SO-DIMM


Intel Gemini Lake Platform

01--COVER PAGE	26--G_SENSORS&HALL
02--BLOCK DIAGRAM	27--RTC
03--POWER BLOCK DIAGRAM	28--AUDIO
04--SYSTEM LIST	29--WLAN
05--GLK_SOC_MEM(CHA)	30--USB3.0
06--GLK_SOC_MEM(CHB)	31--EC ITE8987
07--GLK_SOC (EMMC/SPI/LPC/AUD/PMU)	32--EC ROM &THERMAL SENSOR
08--GLK_SOC(DDI/DSI)	33--HDD
09--GLK_SOC (I2C/CNV/LPSS/SPI/UART)	34--Reserve_FP
10--GLK_SOC (PCIE/SATA/USB)	35--KeyBoard&TouchPad&FAN
11--GLK_SOC (JTAG/GPIO)	36--IO BOARD CONN
12--GLK_SOC (PWR)	37--TPM
13--GLK_SOC (GND)	38--LAN
14--GLK_SOC (DECAP)	39--DCIN&DEBUG CONN
15--GLK_SOC (STRAP)	40--HYBRID CHARGE
16--MEM_SODIMM	41--POWER DELIVERY 3P3V
17--MEM_DDR4_CHA0	42--POWER DELIVERY 5P5V
18--MEM_DDR4_CHA1	43--PMIC RT5077_1
19--DDR4_TERMINATIONS	44--PMIC RT5077_2
20--MEM_DECAPS	45--POWER DELIVERY VDDQ
21--SYSTEM_SPI_FLASH	46--LOAD SWITCH
22--HDMI	47--AC POWER ON SQUENCE 1
23--EDP	48--DC POWER ON SQUENCE 2
24--EMMC	49--POWER DELIVERY_Backlight
25--SSD	50--HOLE&BOSS
	51--CHANGE LIST

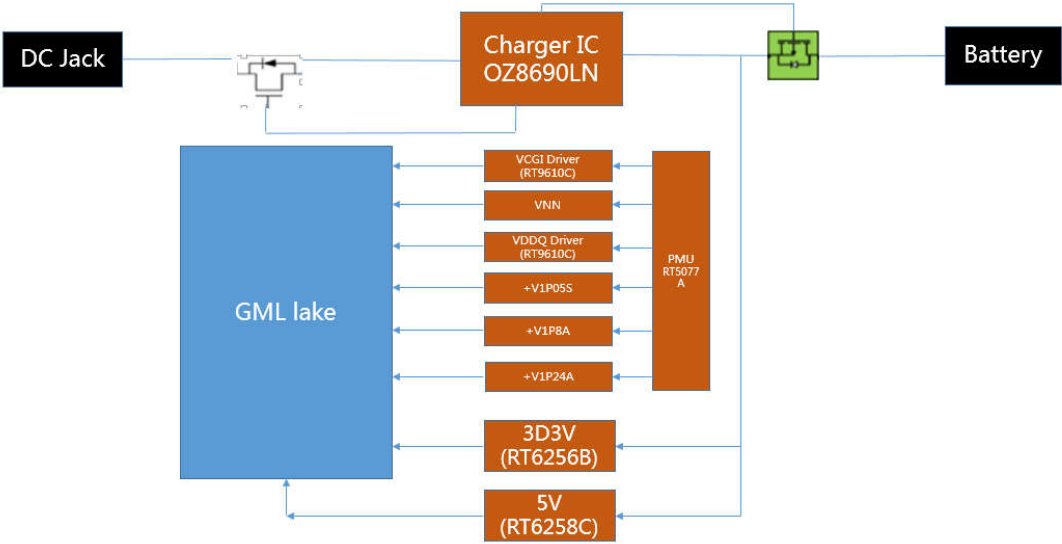
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HQNB0	NB8609	Rev	V1.0
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Power States(Adapter)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGI	V1P05S	+V1P20_VDDQ	+3P3SX	+1P8SX	+5P0SX	+V3P3SX_OPS
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON/OFF ²
S4(STD)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ²
S5(SoftOff)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ²

Notel:CNVi moudle on,Pcie moudle off

Power States(Battery)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGI	V1P05S	+V1P20_VDDQ	+3P3SX	+1P8SX	+5P0SX	+V3P3SX_OPS
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON/OFF ²
S4(STD)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ²
S5(SoftOff)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ²

Notel:CNVi moudle on,Pcie moudle off

MEM ID

MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	4x HYNIX 1GB (H5AN8G6NCJR-VXC)
0	0	1	4x Micron 1GB (MT40A512M16LY-075:E)
0	1	0	4x Micron 1GB (MT40A512M16TB-062E:J)
0	1	1	xxx
1	0	0	xxx
1	0	1	xxx

MB ID

			HW_ID6	HW_ID5	HW_ID2	HW_ID1	HW_ID0
	EVT		X	X	1	1	1
NB8609	DVT						
NB8612	DVT						

PCle Port

Port	Device
0-3	SSD
4	LAN
5	WLAN

SATA Port

Port	Device
0	HDD
1	SSD

USB2.0 Port

Port	Device
0	USB2.0 Type-A
1	USB3.0 Type-A
2	USB2.0 Type-A(DB)
4	BT
5	Touch screen
6	Camera

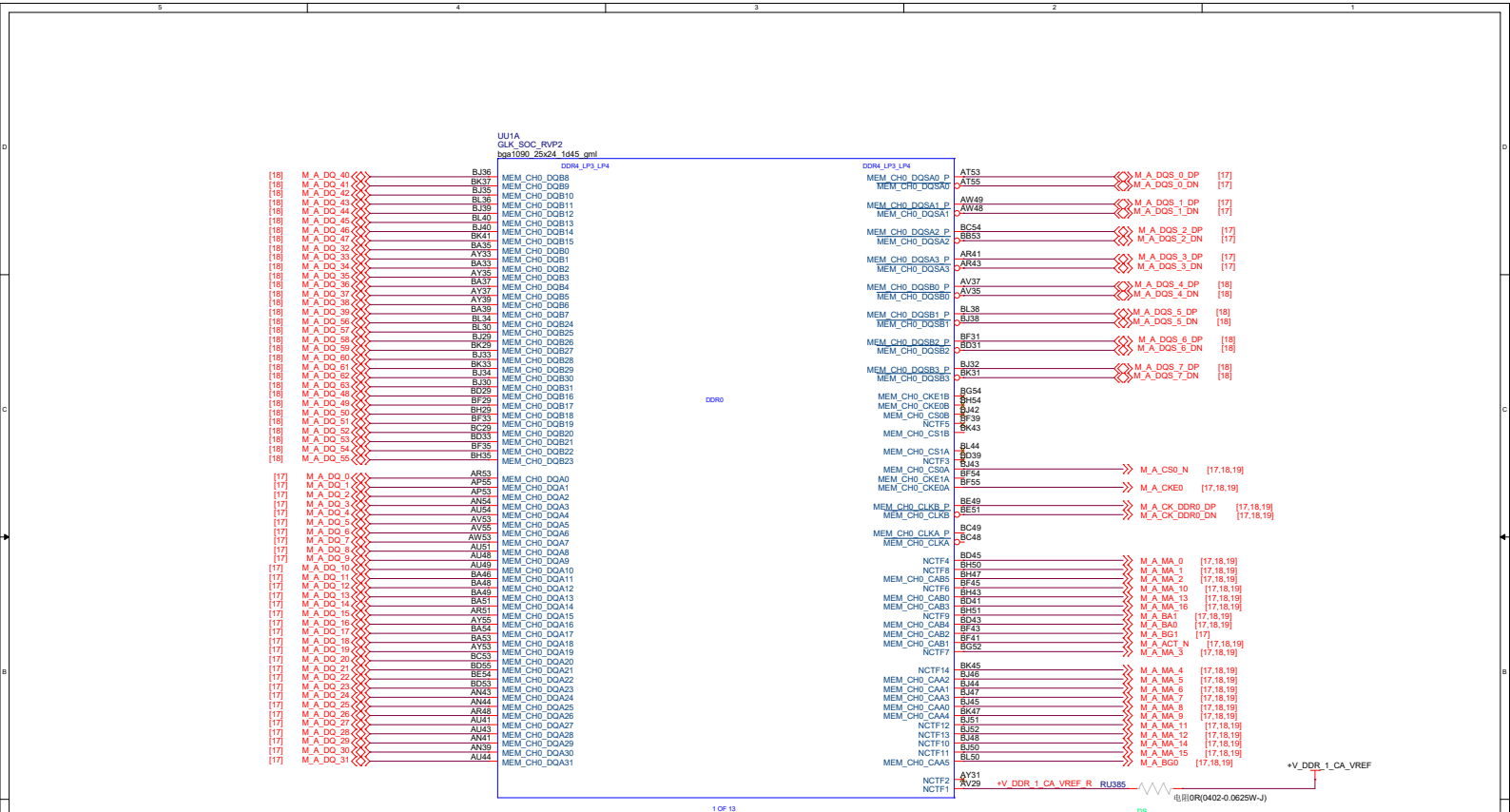
USB3.0 Port


Port	Device
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1	NA



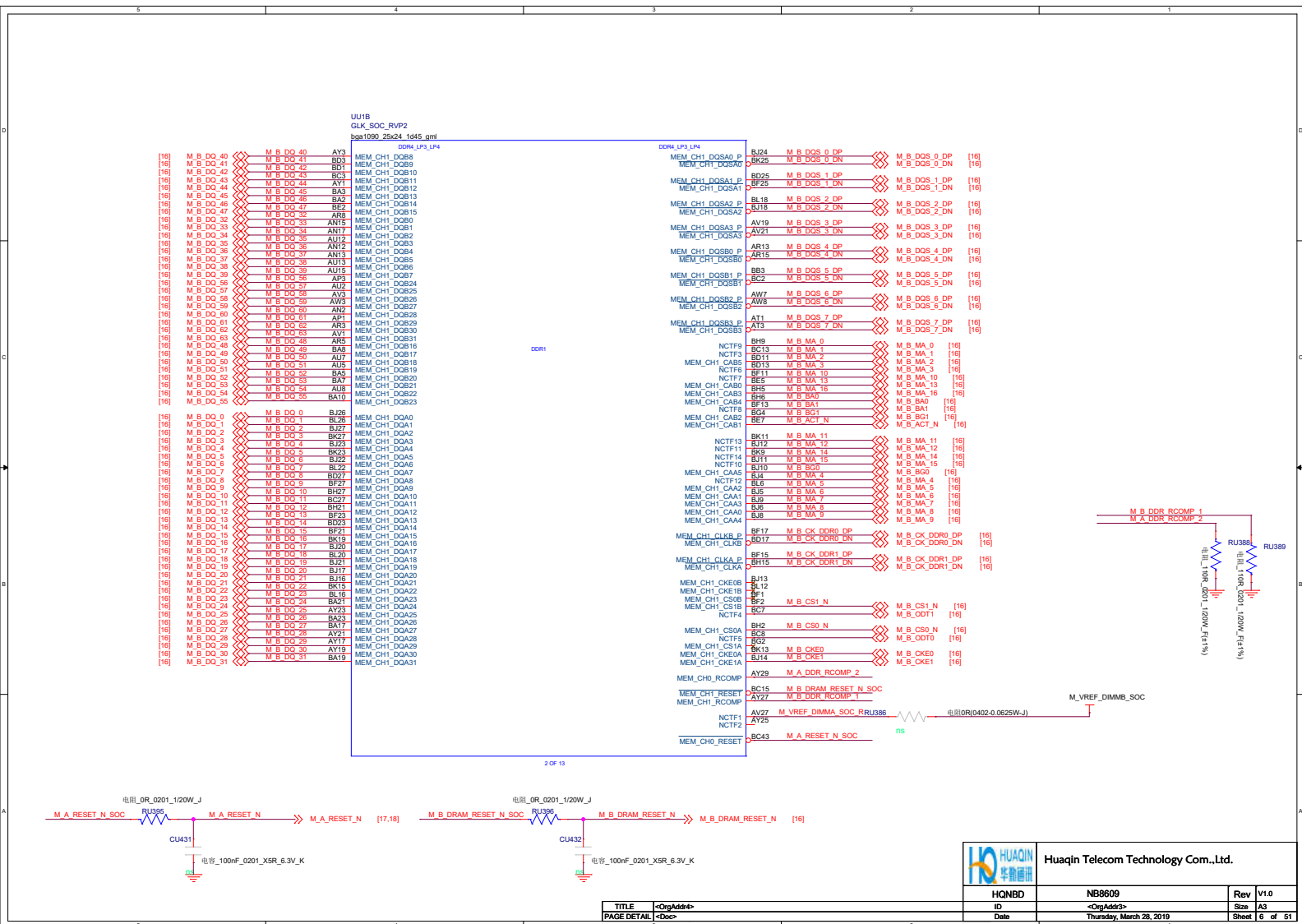
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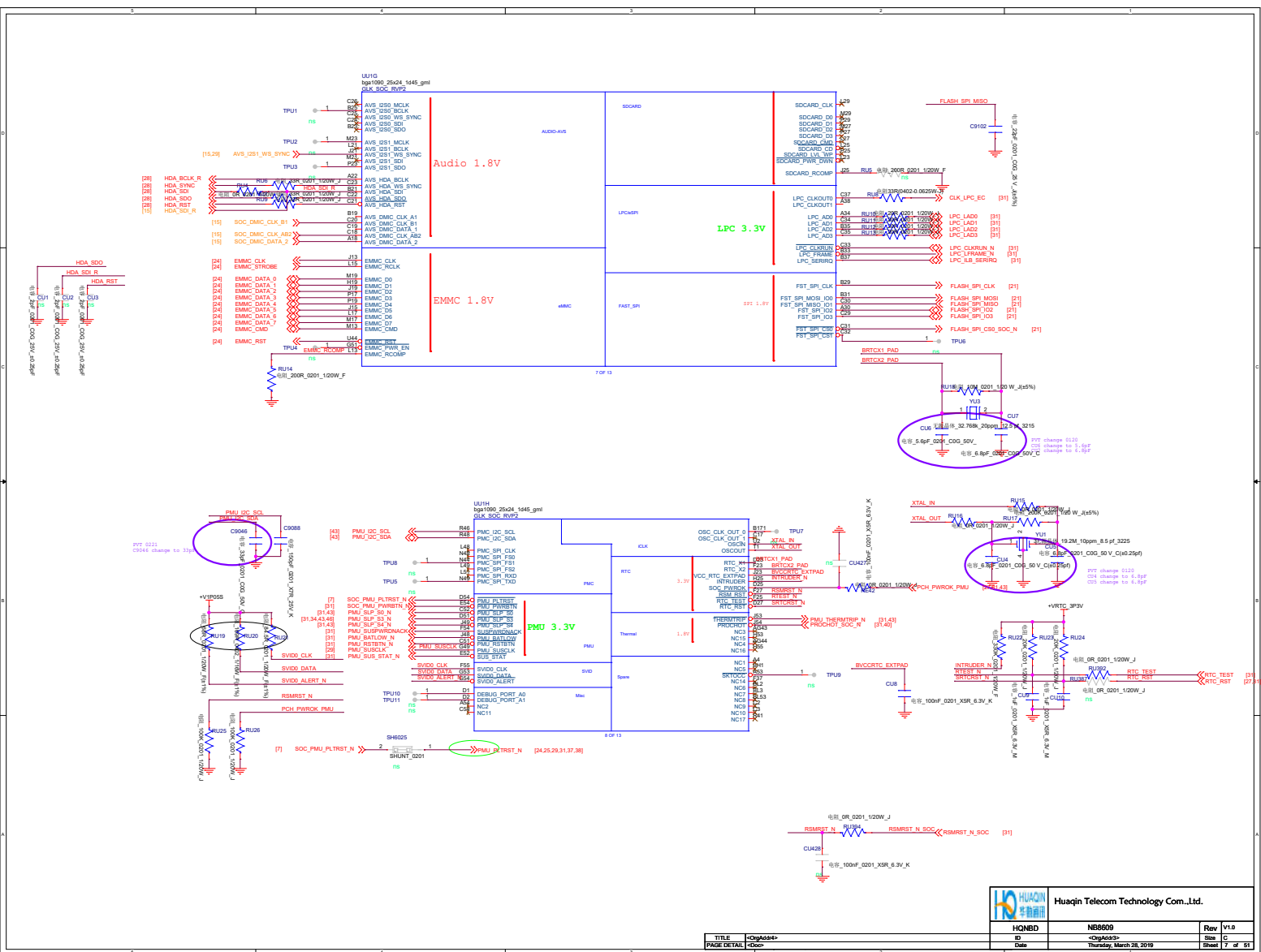
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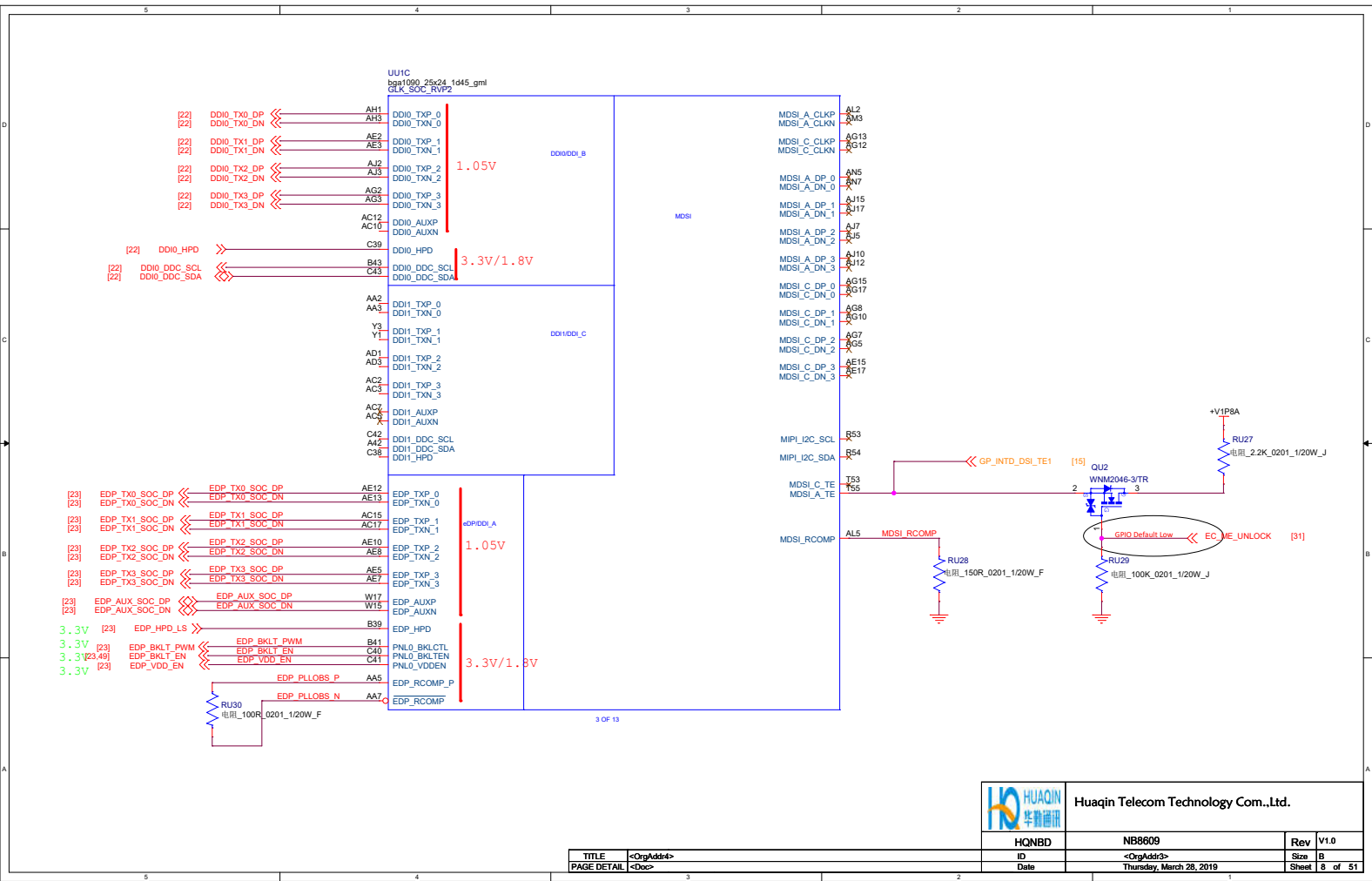


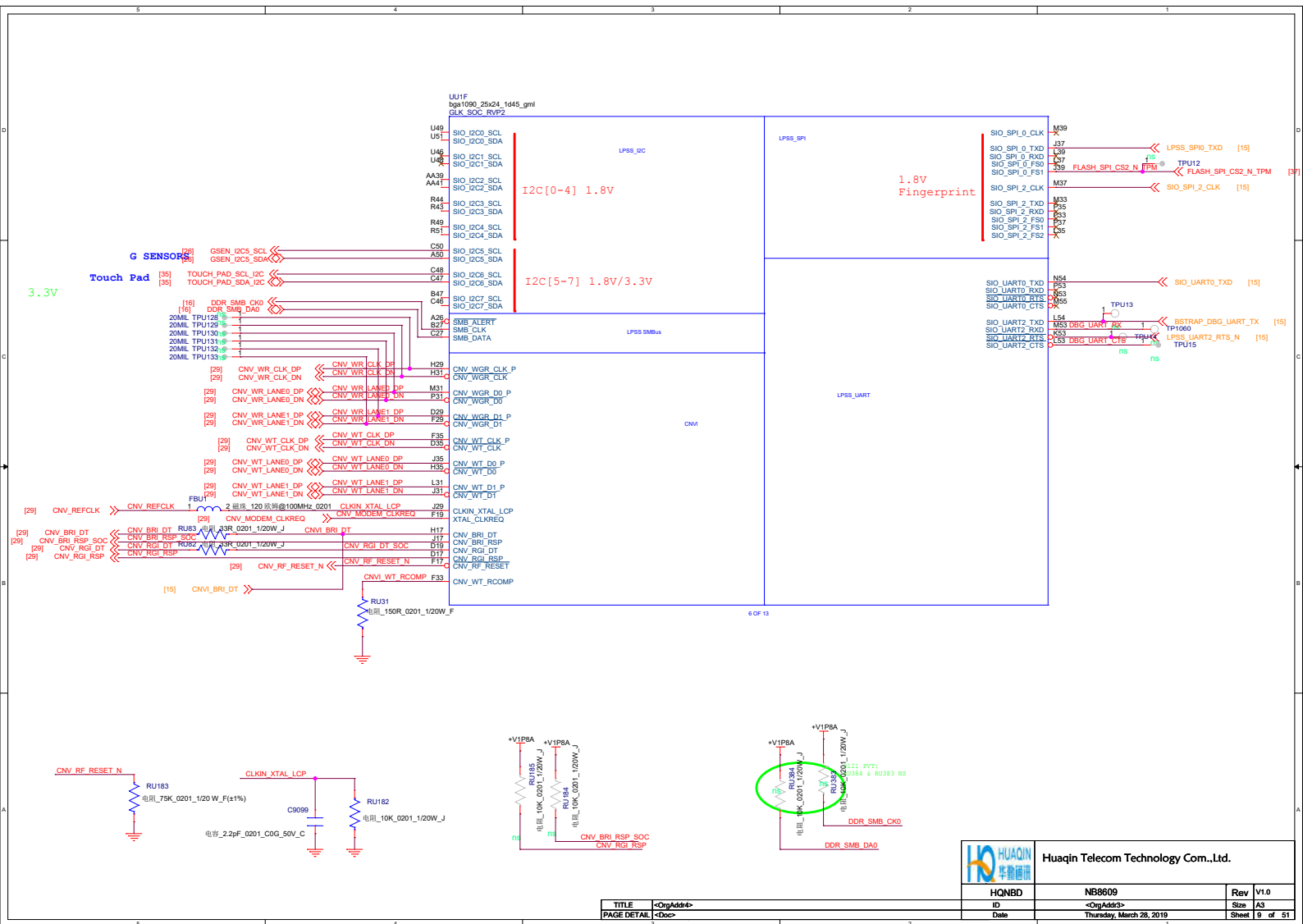
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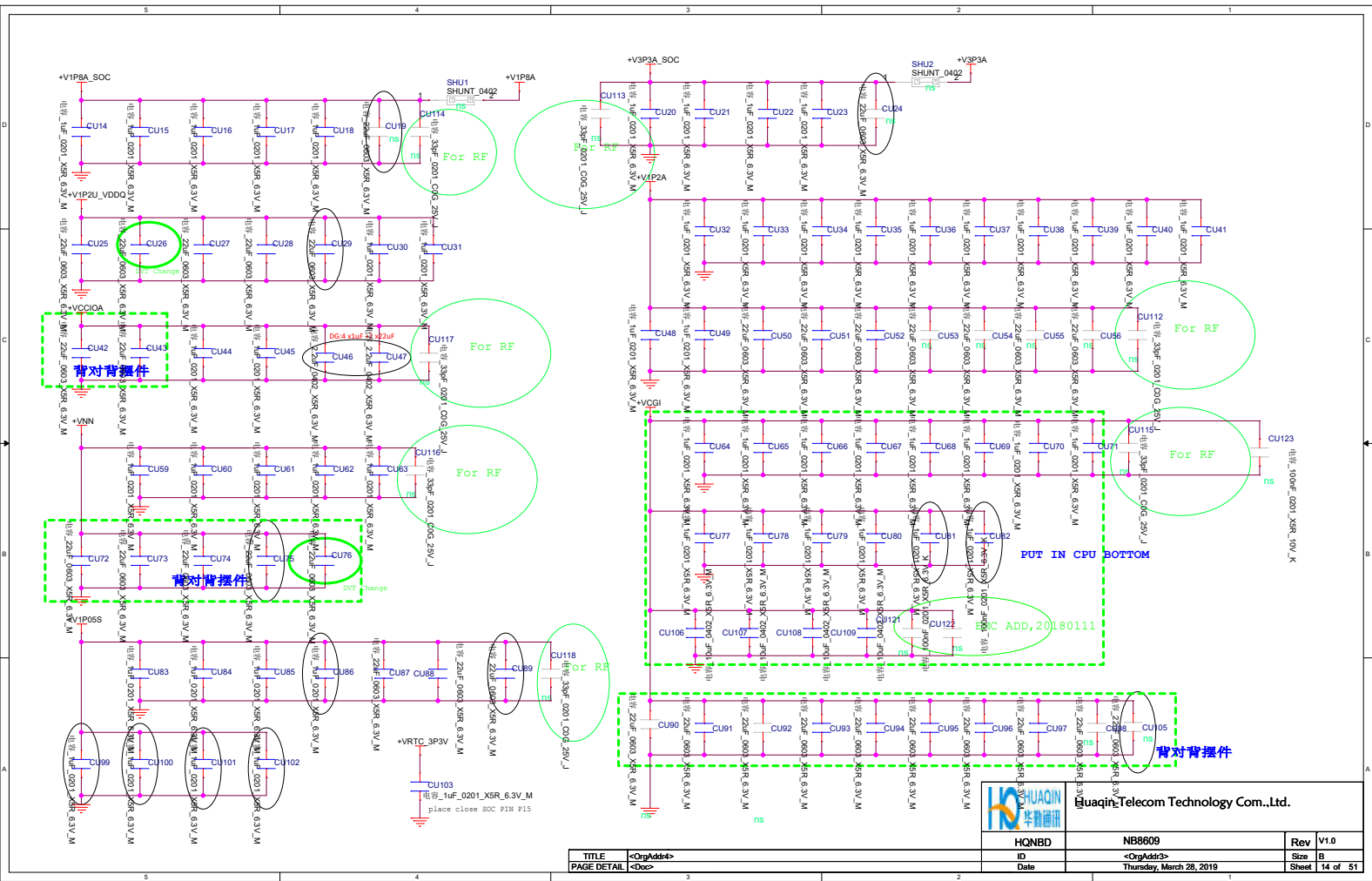








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A6	VSS13		VSS54	AF47					
A12	VSS1		VSS55	AF48					
A16	VSS2		VSS56	AF50					
A24	VSS3		VSS57	AF52					
A34	VSS4		VSS58	AF53					
A38	VSS5		VSS59	AF55					
A39	VSS7		VSS60	AG20					
VSS8			VSS64	AL21					
A40	VSS8		VSS67	AK25					
A44	VSS9		VSS65	AG29					
A48	VSS10		VSS66	AG35					
A51	VSS11		VSS67	AG38					
AA12	VSS12		VSS68	AJ8					
AA13	VSS14		VSS77	AJ13					
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AA35	VSS21		VSS75	AJ44					
AA43	VSS22		VSS76	AK1					
AA48	VSS23		VSS78	AK3					
AB1	VSS24		VSS79	AK55					
AB3	VSS25		VSS80	AL3					
AB55	VSS26		VSS90	AL7					
AC8	VSS27		VSS97	AL8					
AC13	VSS33		VSS98	AL10					
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AF3	VSS49		VSS95	AL51					
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AF6	VSS62		VSS100	AM21					
AF9	VSS63		VSS101	AM25					
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AF12	VSS42		VSS103	AM31					
AF14	VSS43		VSS104	AM38					
AF16	VSS44		VSS105	AM55					
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AF42	VSS52								
11 OF 13									
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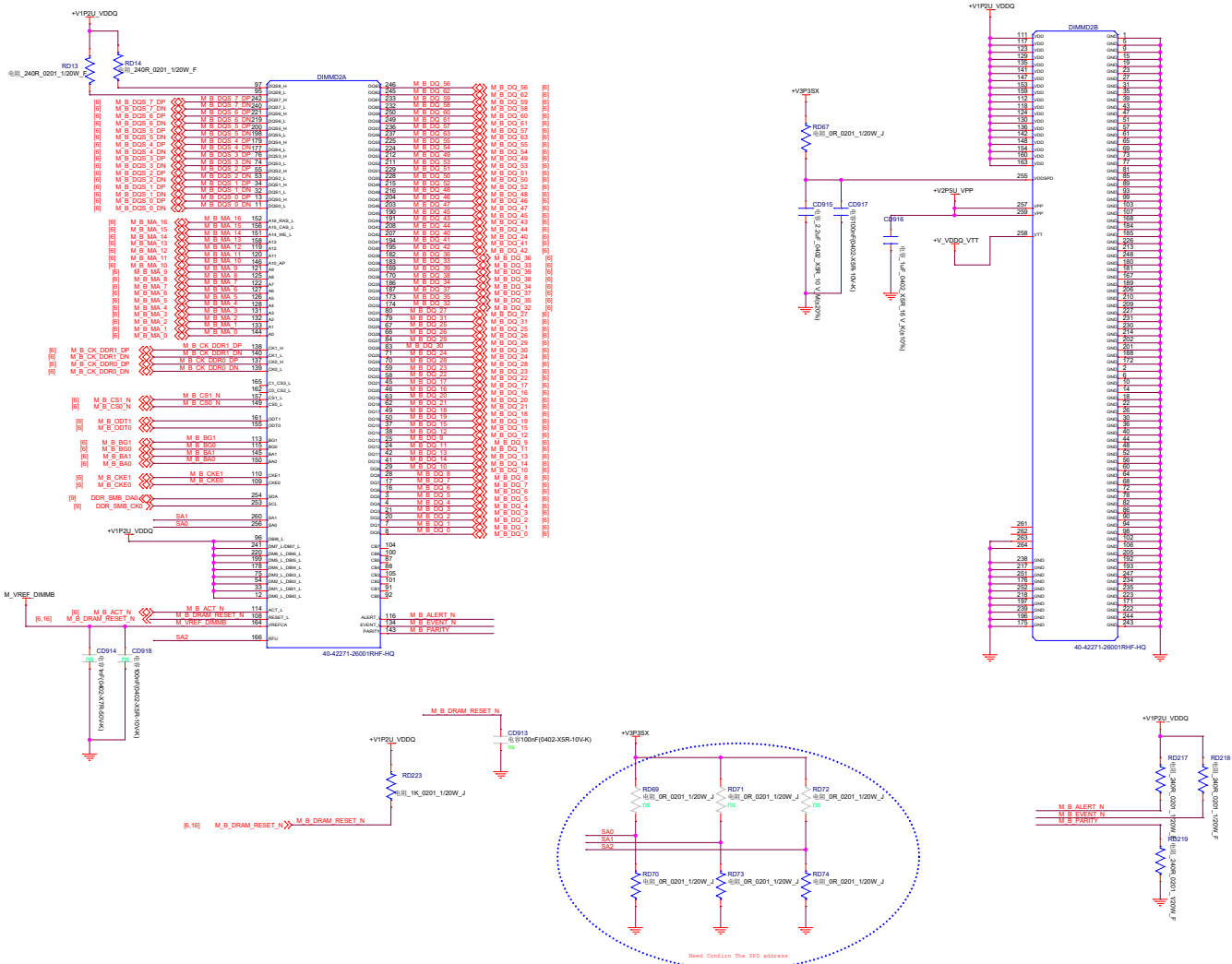


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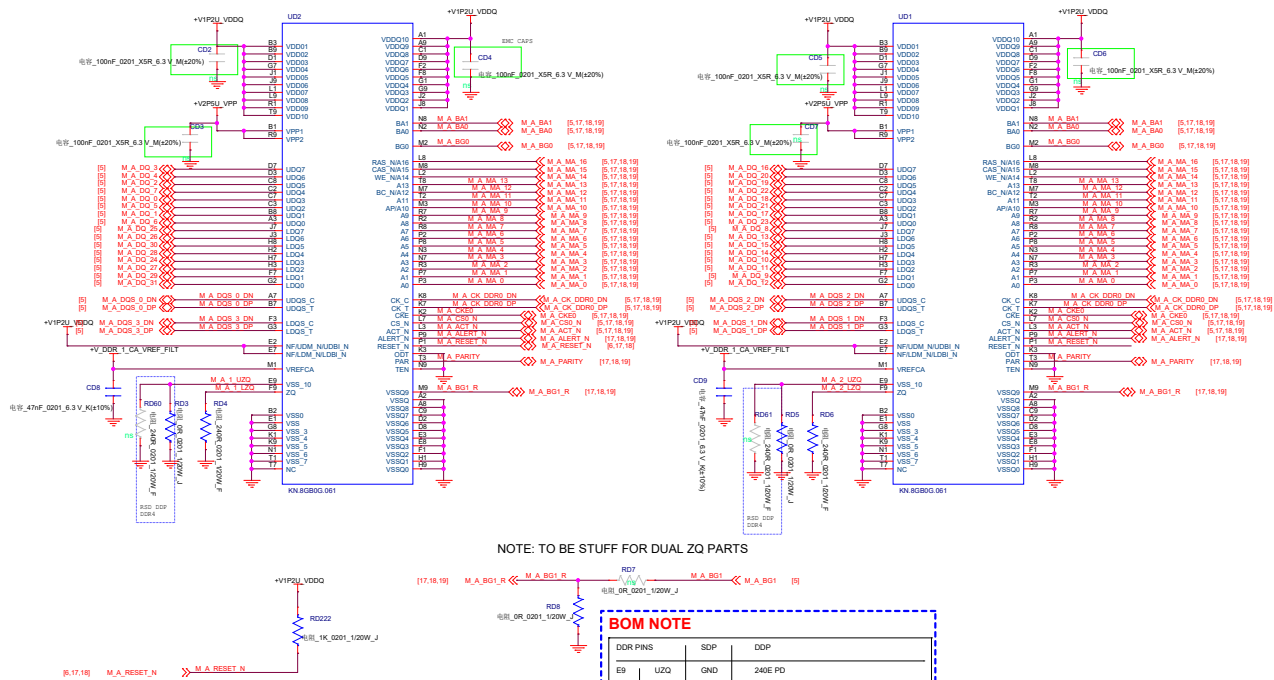
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Thursday, March 28, 2019

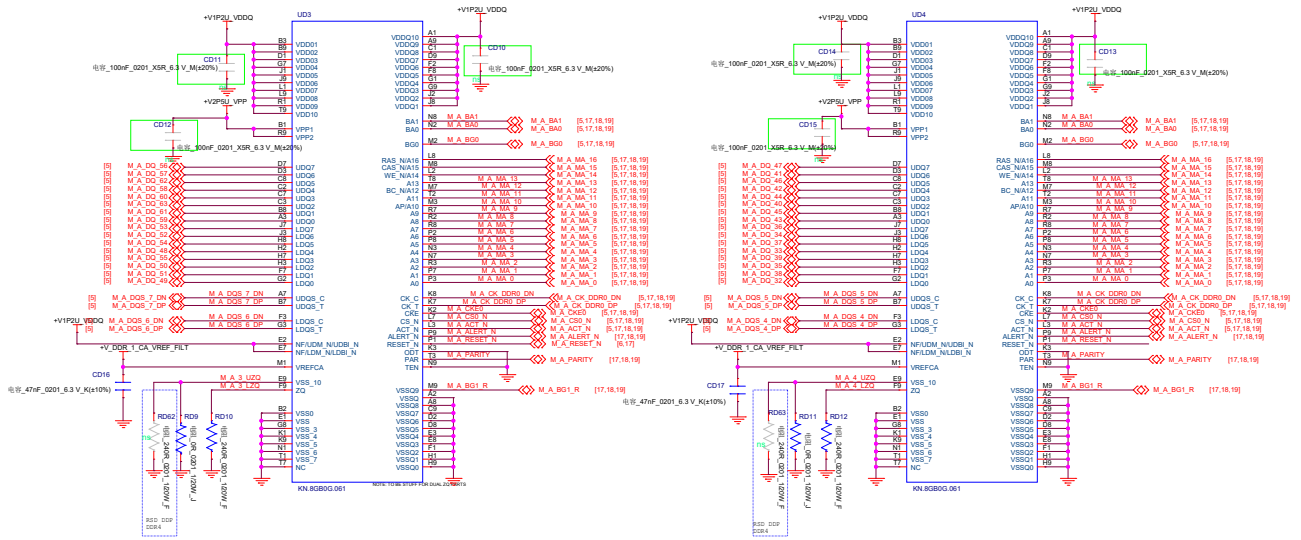
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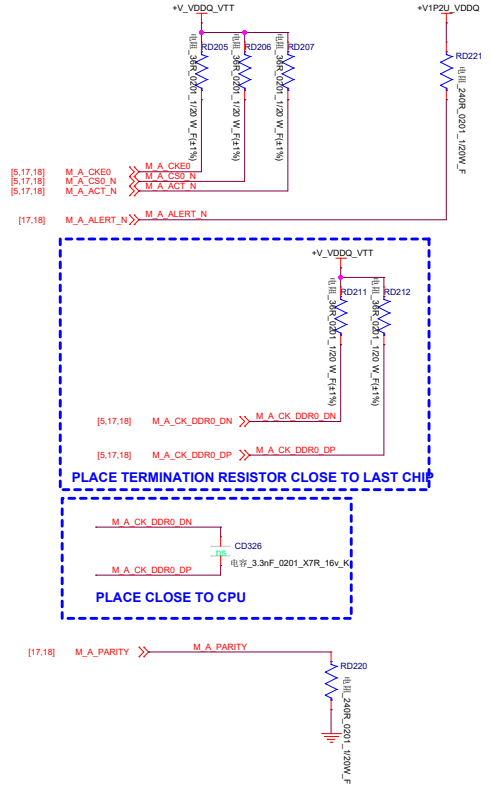
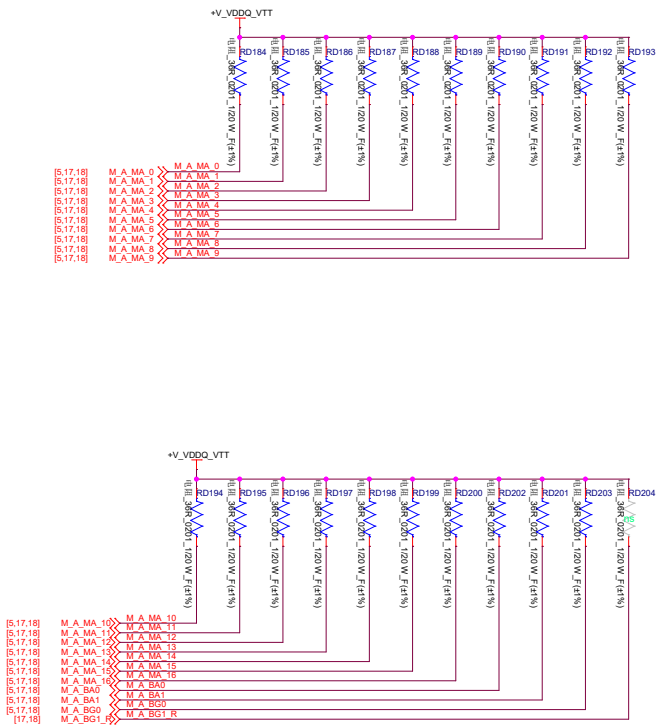
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MEMORY TERMINATIONS MD CHANNEL A

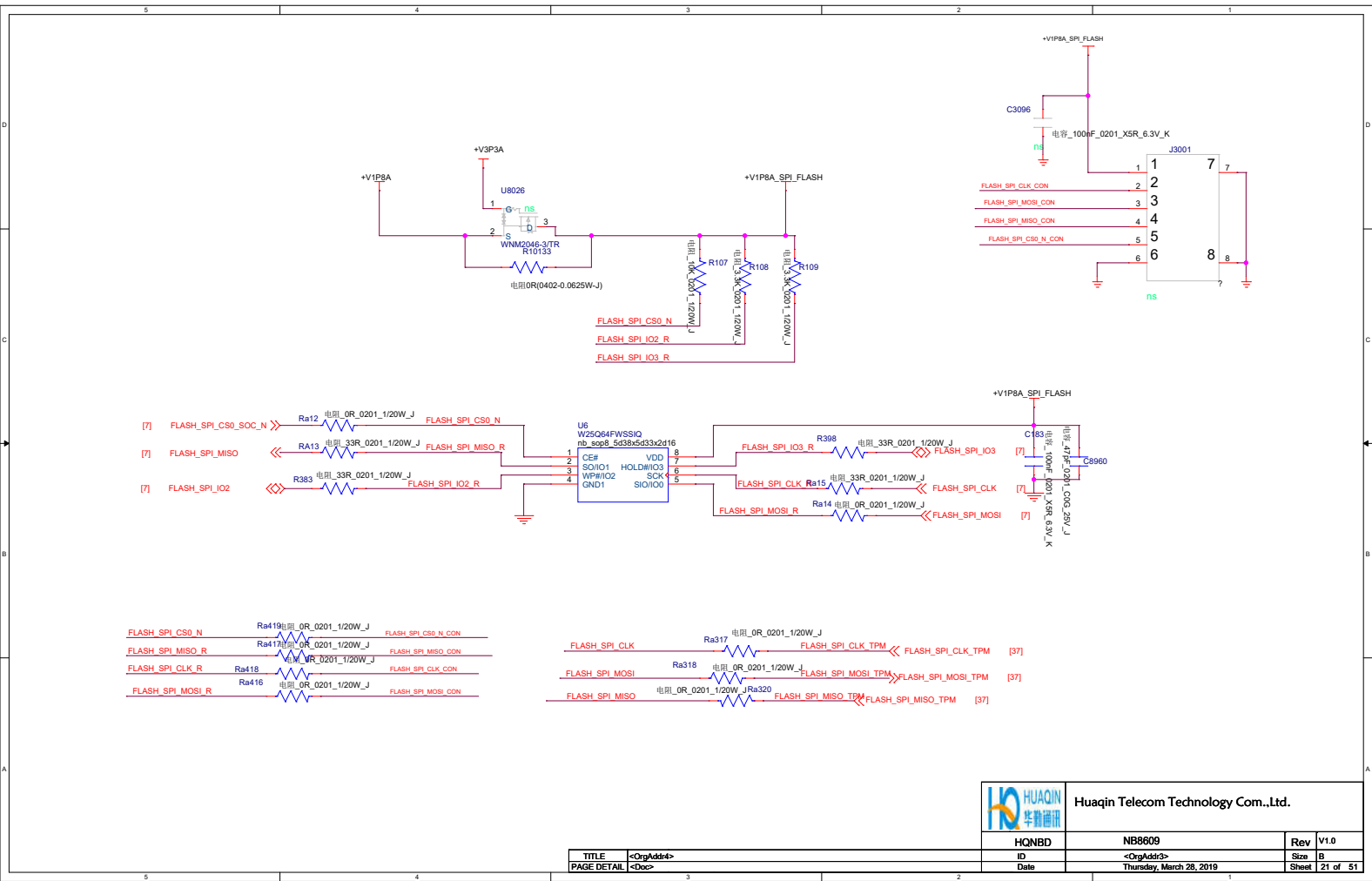



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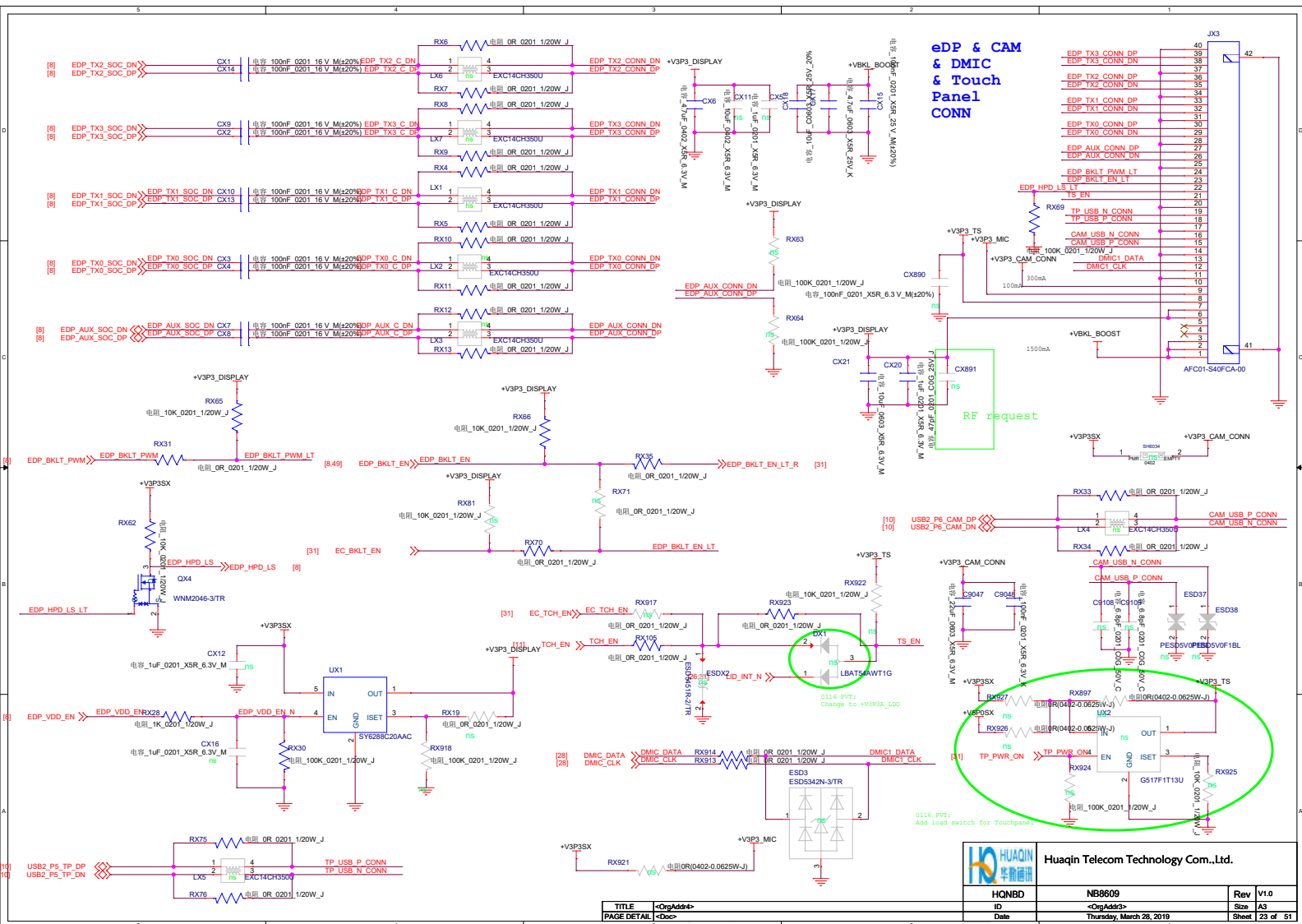
The diagram illustrates a differential signal path. It starts with a supply voltage $VPP33_VDDO$ connected to a resistor $RD64$ (labeled $10k$). This resistor is connected to a node that branches into two paths: one through resistor $RD65$ (labeled $3.69k$) to a node labeled M_VREF_OCMAMB , and another through resistor $RD66$ (labeled 201) to a node labeled $M_VREF_DMAMB_SOC$. Both M_VREF_OCMAMB and $M_VREF_DMAMB_SOC$ are connected to a common node that then branches into two paths: one through resistor $RD67$ (labeled $100k$) to a node labeled $M_VREF_DMAMB_SOC$, and another through resistor $RD68$ (labeled $10k$) to a node labeled $M_VREF_DMAMB_SOC$. The final output is a differential signal labeled $M_VREF_DMAMB_SOC$ and $M_VREF_DMAMB_SOC$ (with a note $100k$ and $10k$ in parentheses). The resistors are labeled with values like $10k$, $3.69k$, 201 , $120W_F$, and $100k$.


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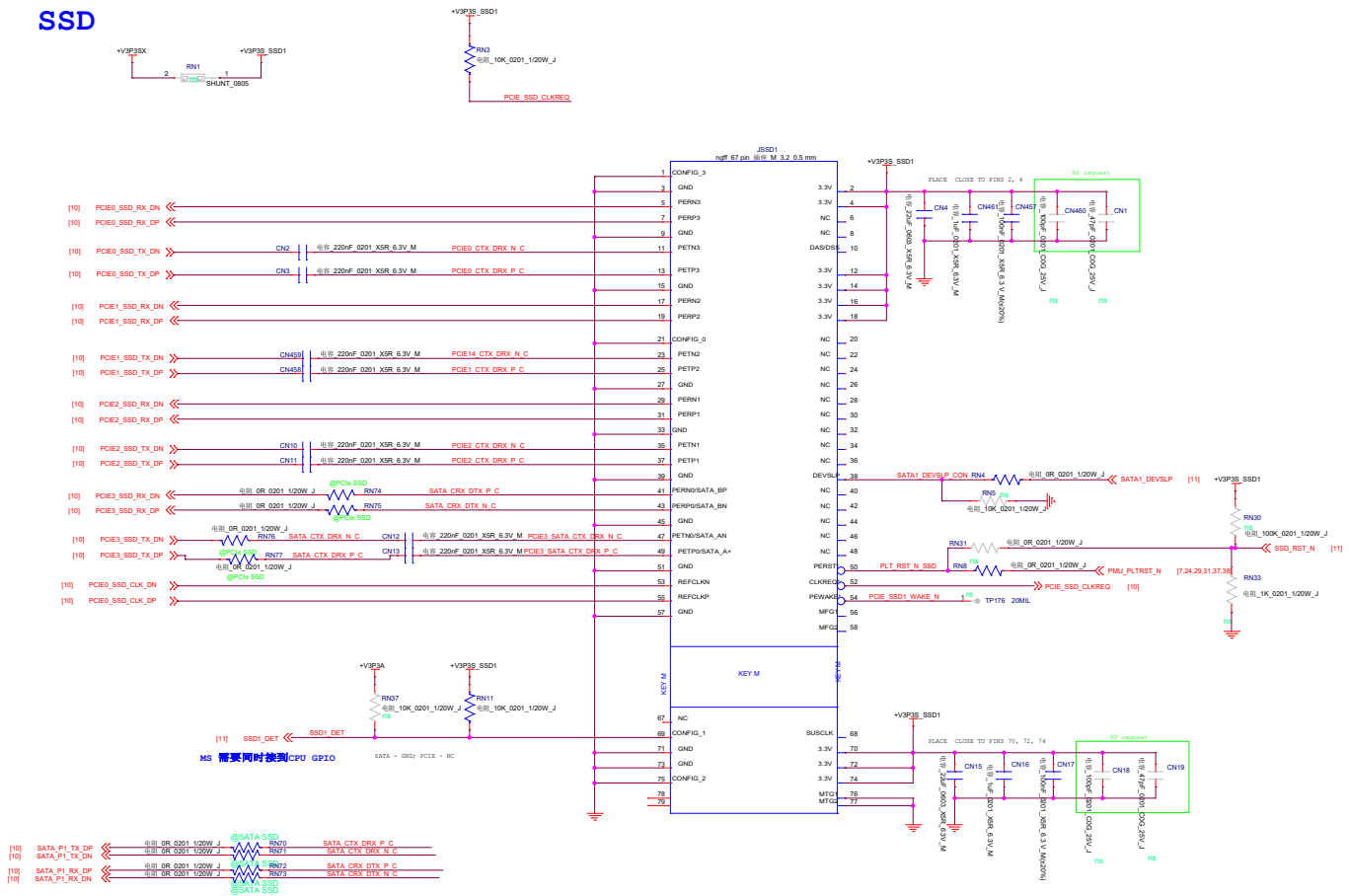
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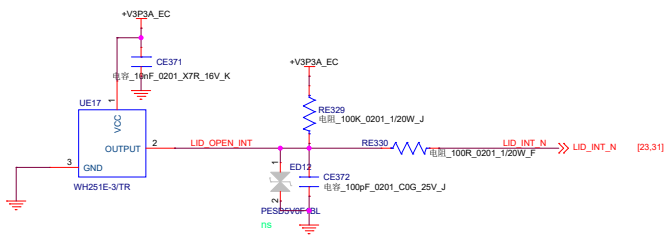
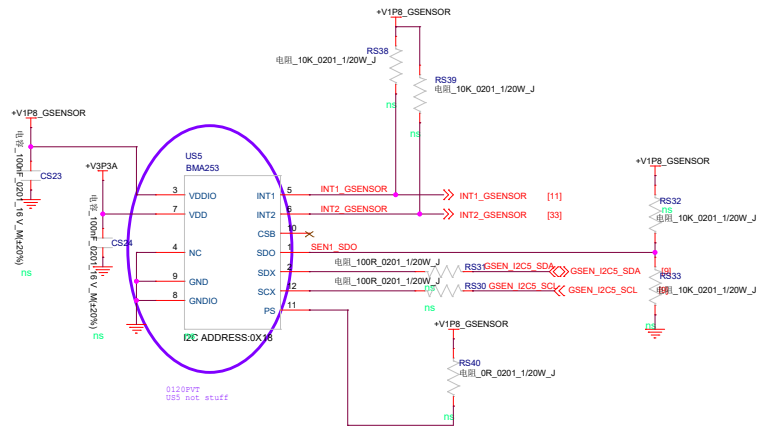
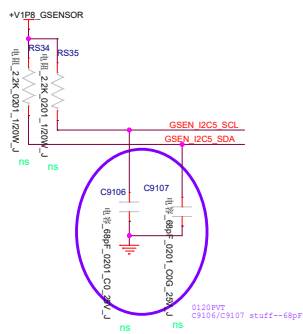
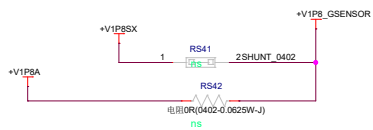
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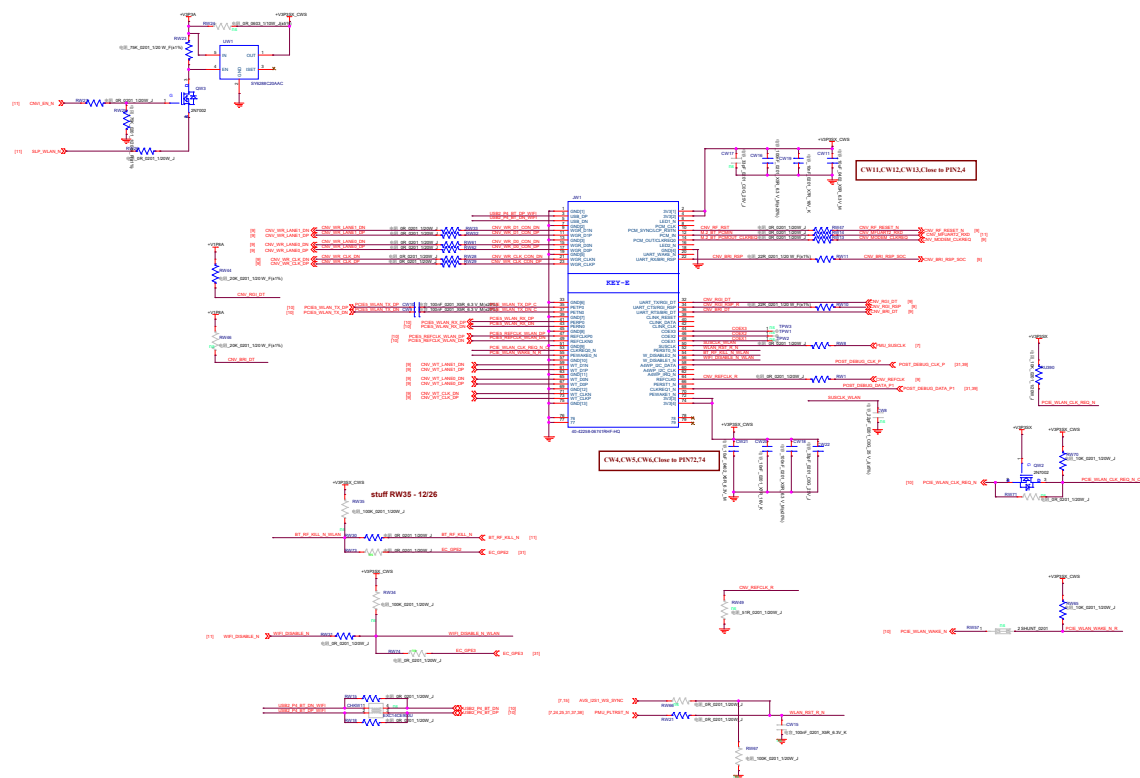
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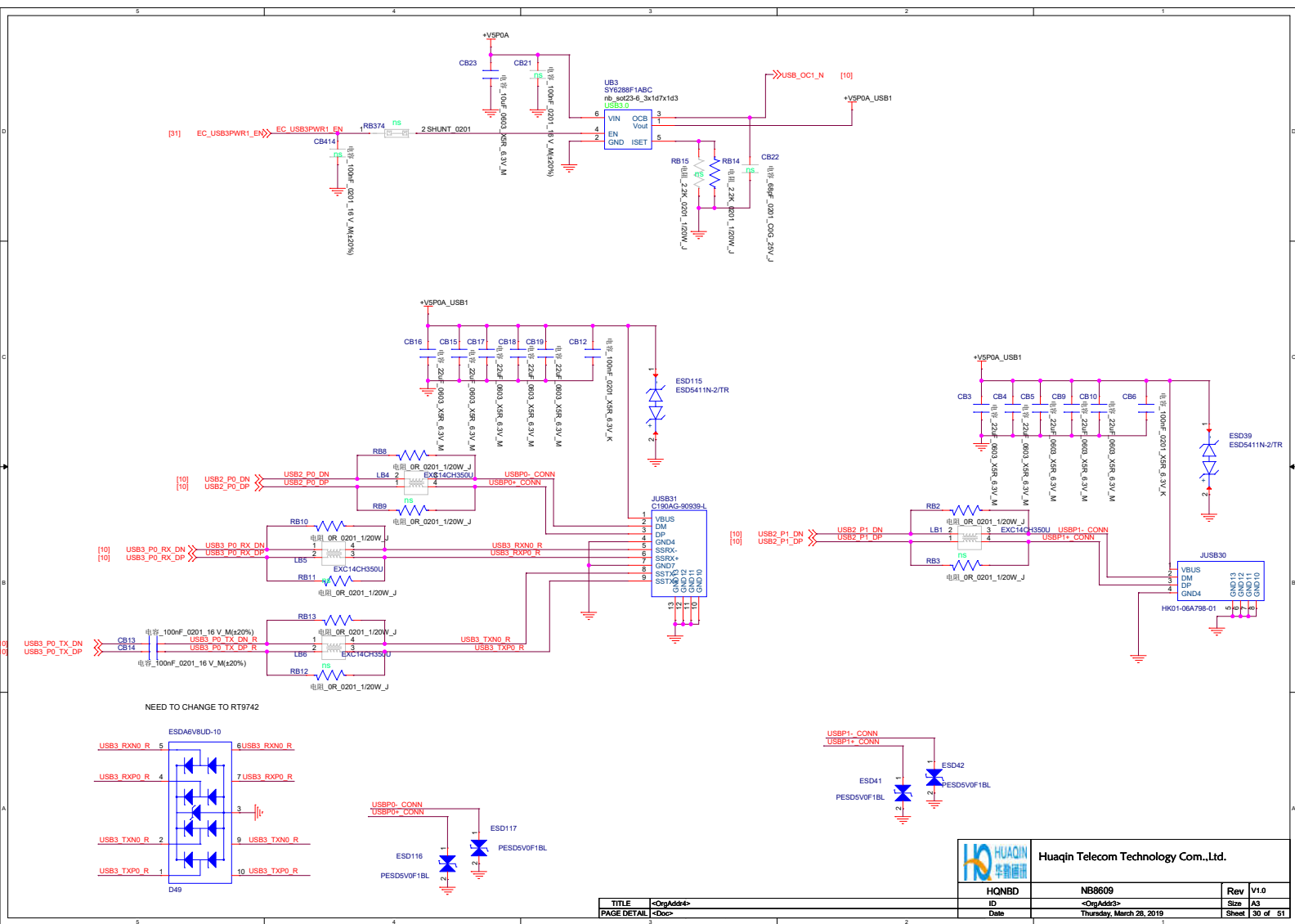




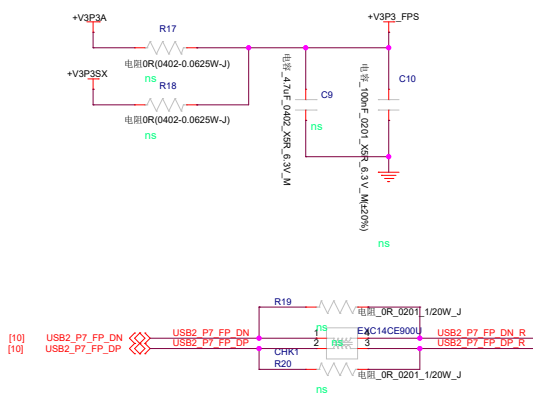
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HQNB01	NB8609	Rev	V1.0
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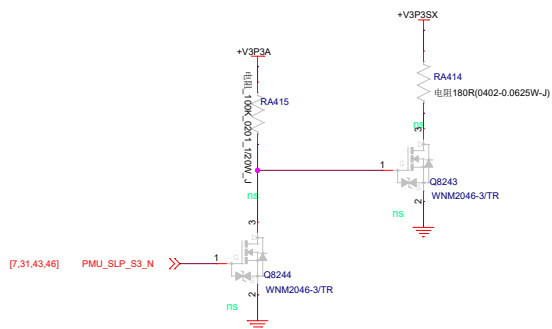
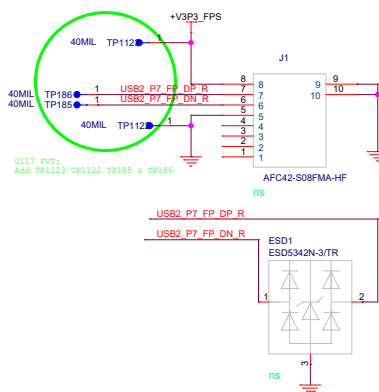





Finger Print

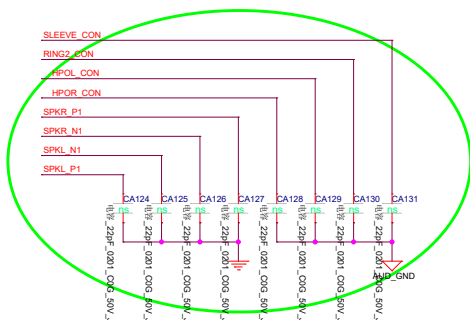


Finger Print CONN

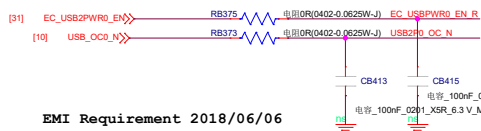


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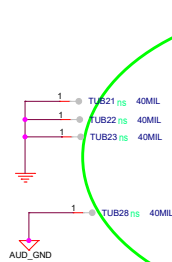
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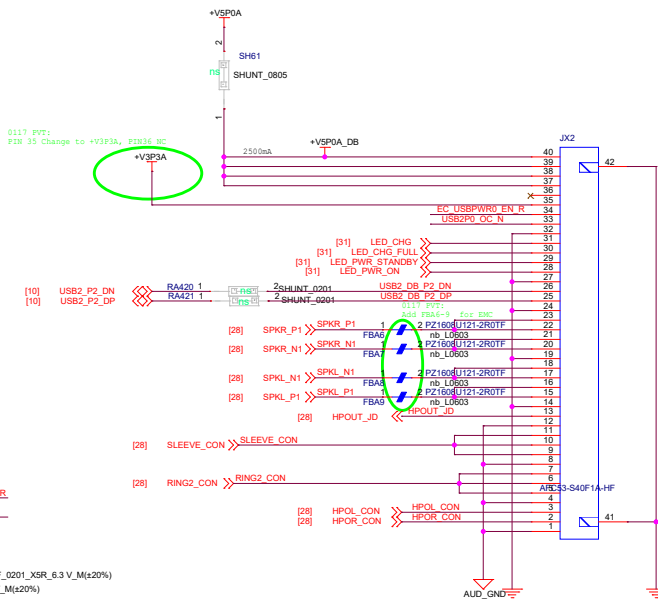
0117 FVT:
Add CA124 CA125 CA126 CA127 CA128 CA129 CA130 CA131 for GND



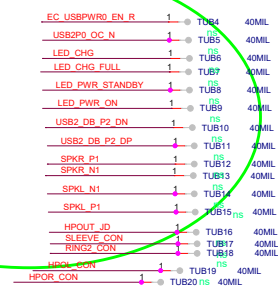
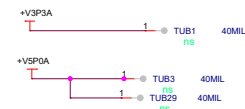
EMI Requirement 2018/06/06




0121 FVT:
Add TP 10 Board for huabei

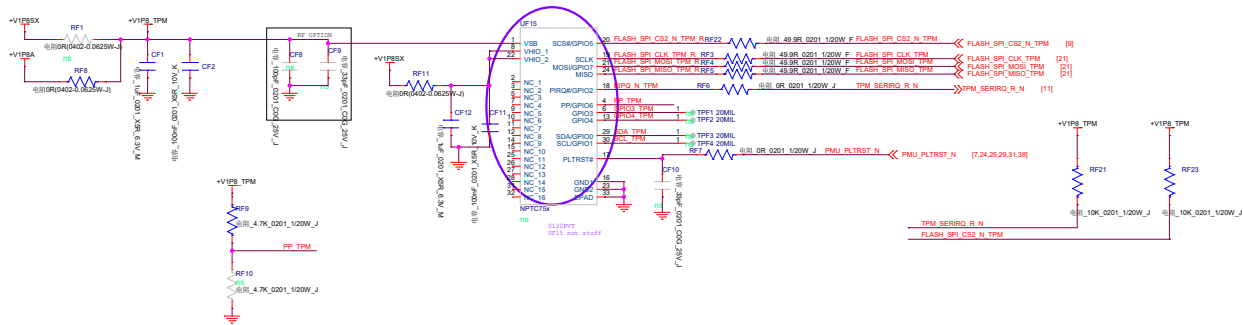



0117 FVT:
PIN 35 Change to +V3P3A, PIN16 NC



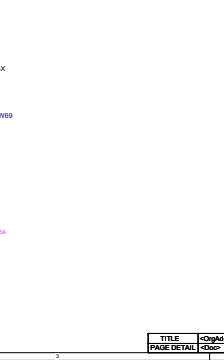
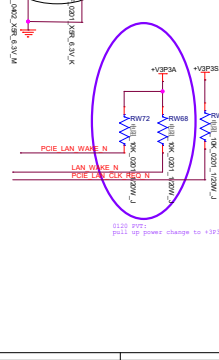
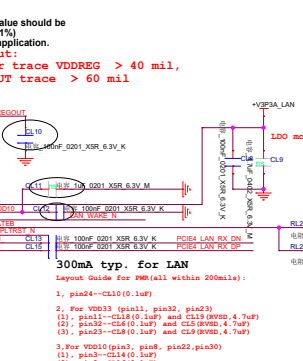
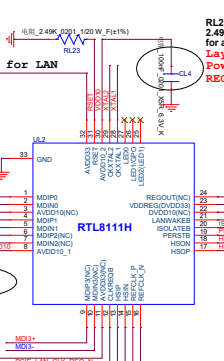
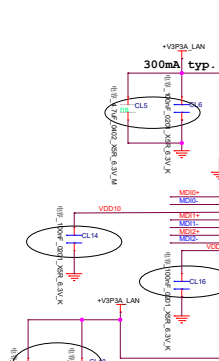
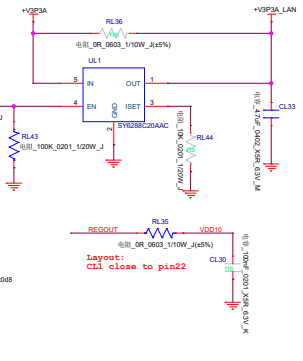
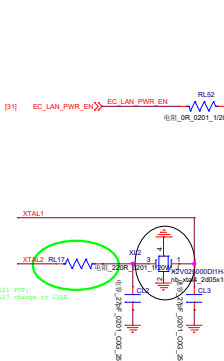
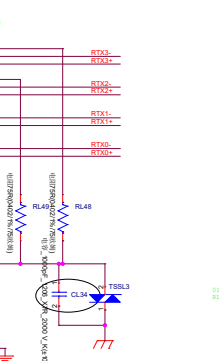
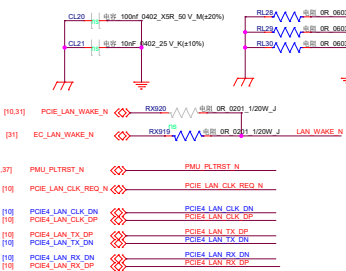
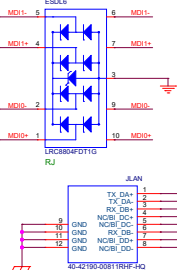
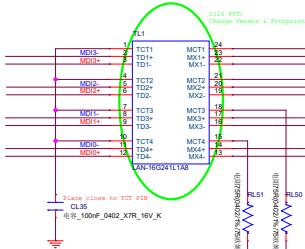
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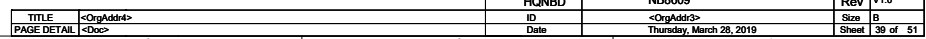
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HC1800	NB9000	Rev	V1.0
Q1	Q1	Rev	1.0
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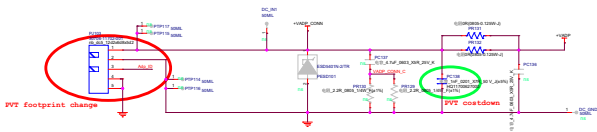


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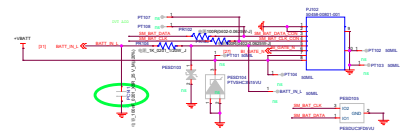
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PAGE DETAIL	Doc



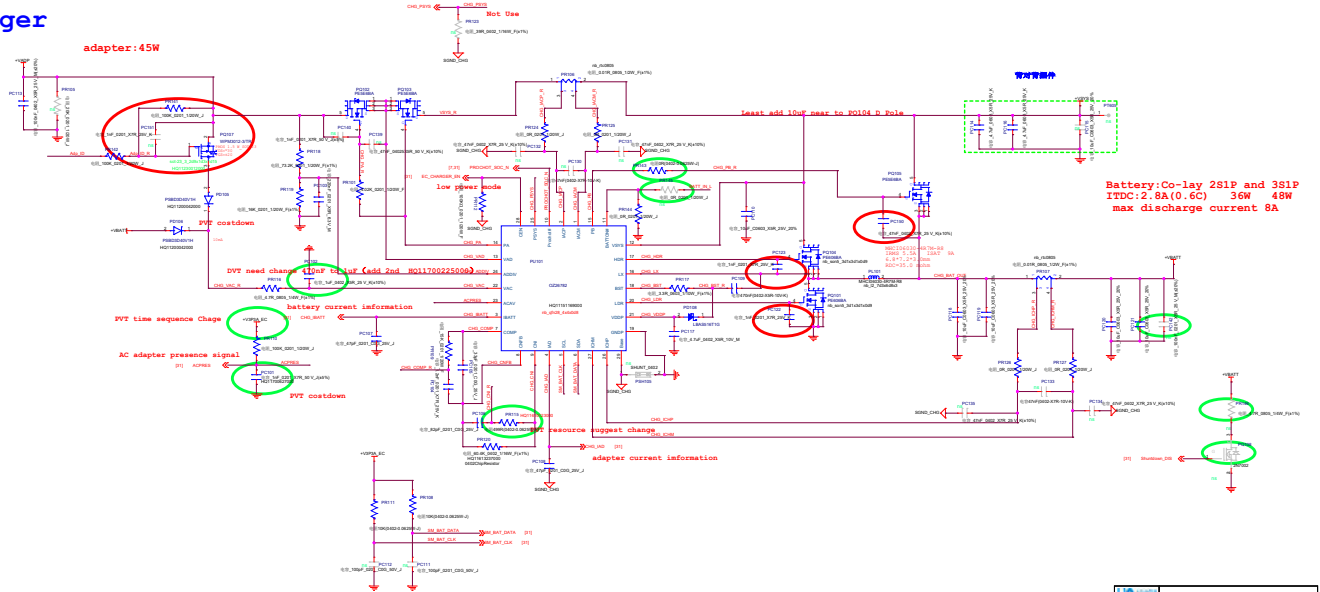
DC IN



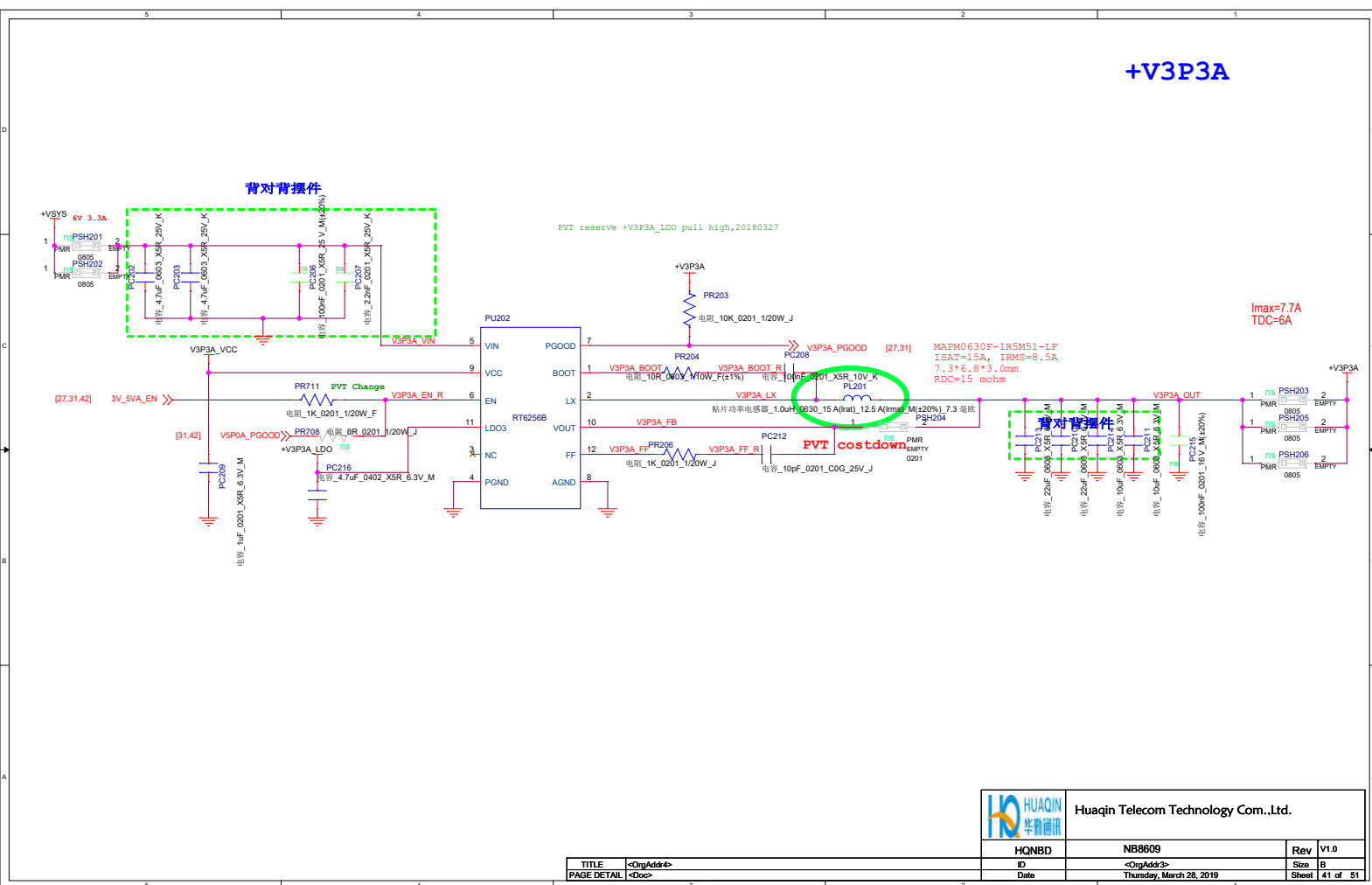
Battery CONN



Charger



Haishin Telecom Technology Co., Ltd.			
Model	Project	Rev	Ver
010001	010001	01	01
01	01	01	01



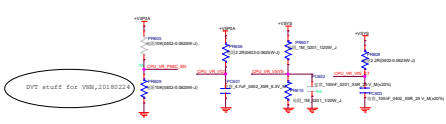
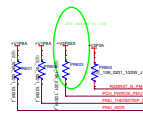
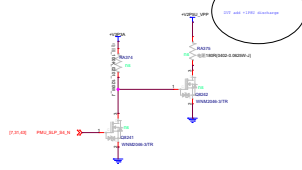
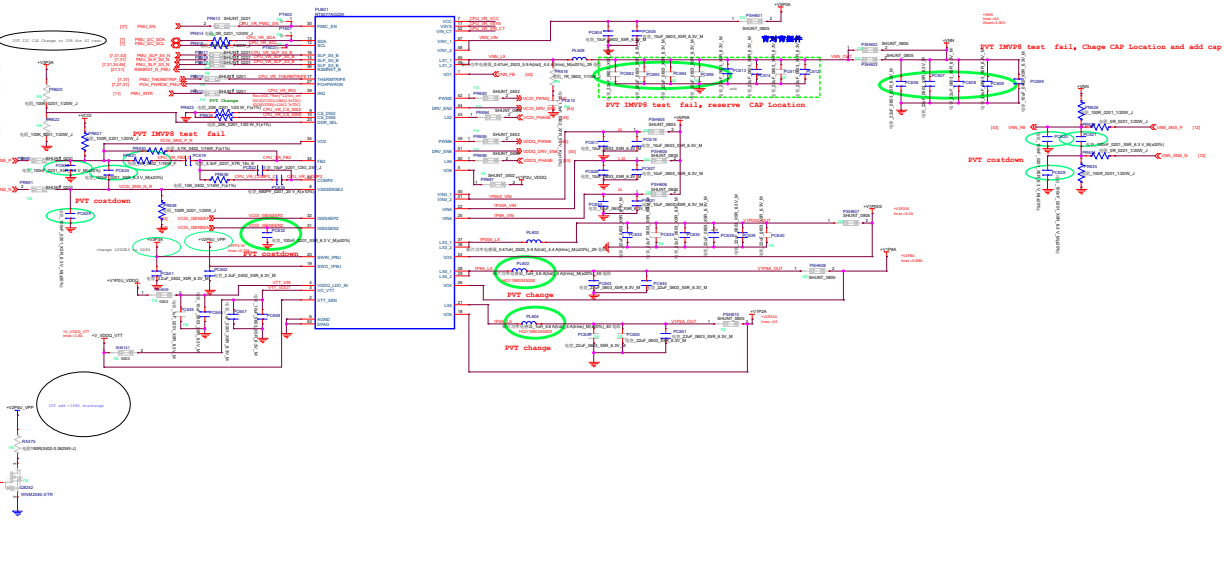


Table 2. Buck2 (DDR) Voltage Selection

DDR_SEL Pin State	Buck2 Nominal Output Voltage	DDR Technology
H	1.2V	LPDDR3
Floating	1.2V	DDR4 (optional)
L	1.1V	LPDDR4



VCGI

+VCGI
Imax = 25A
Vboot=0V

can reduce 3 pos cap not add costdown plan

PRT601 Close to choke

HUAQIN 华勤通信		Huaqin Telecom Technology Com.,Ltd.	
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TITLE	PCBAsses
DATE	2019-03-28
DESIGNER	Wang
CHECKER	Wang
DATE	2019-03-28

VDDQ

IMAX: 8.9A



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Date

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V3P3SX V5P0SX V1P8SX

ITDC:1000mA

ID=6A, RDS (ON) =17mΩ

IMAX:3.72A

PVT costdown

IMAX:2.75A

PVT costdown

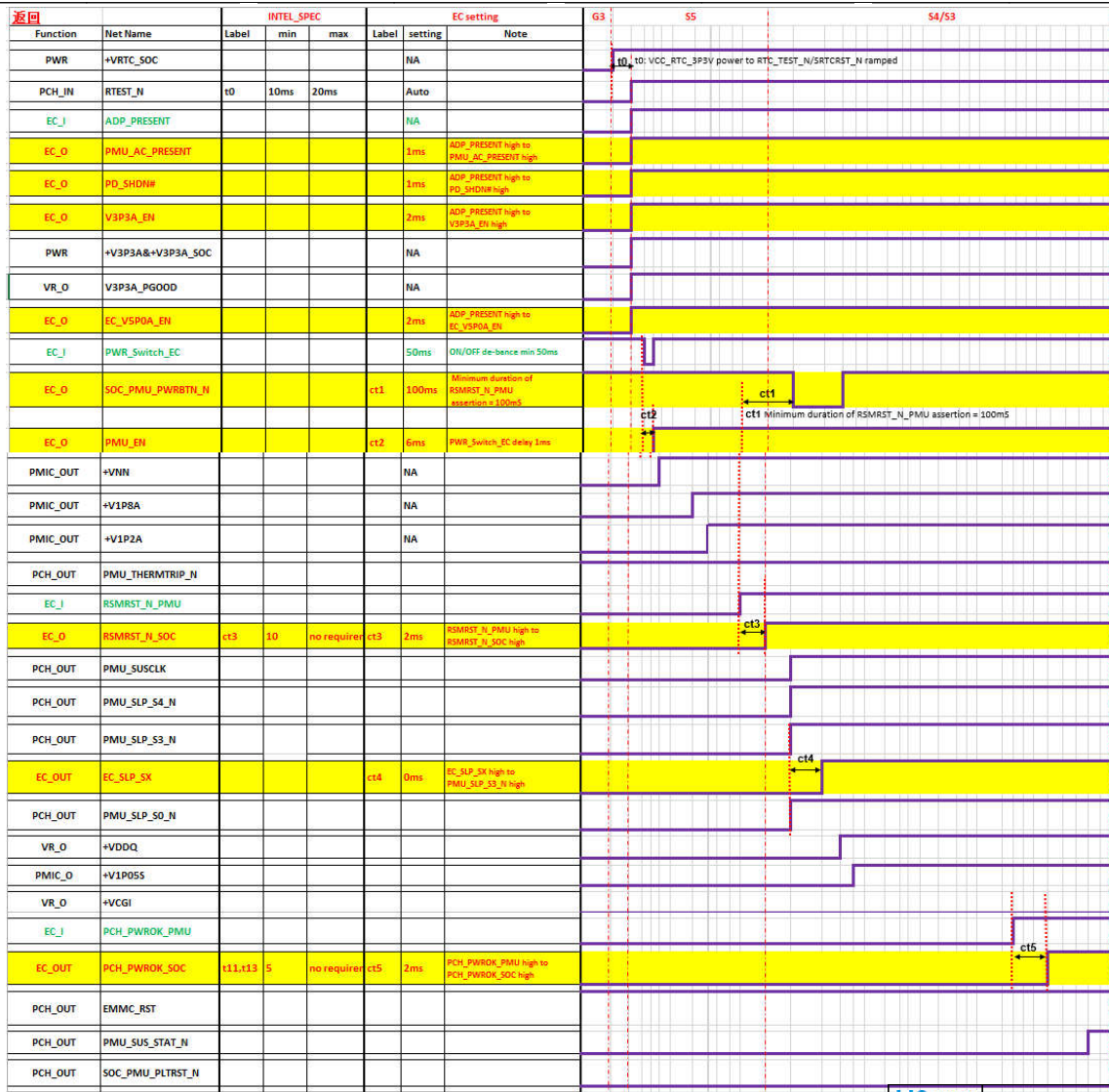
PVT costdown



Huaqin Telecom Technology Co.,Ltd.

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1



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4

3

2

1

D

C

B

A

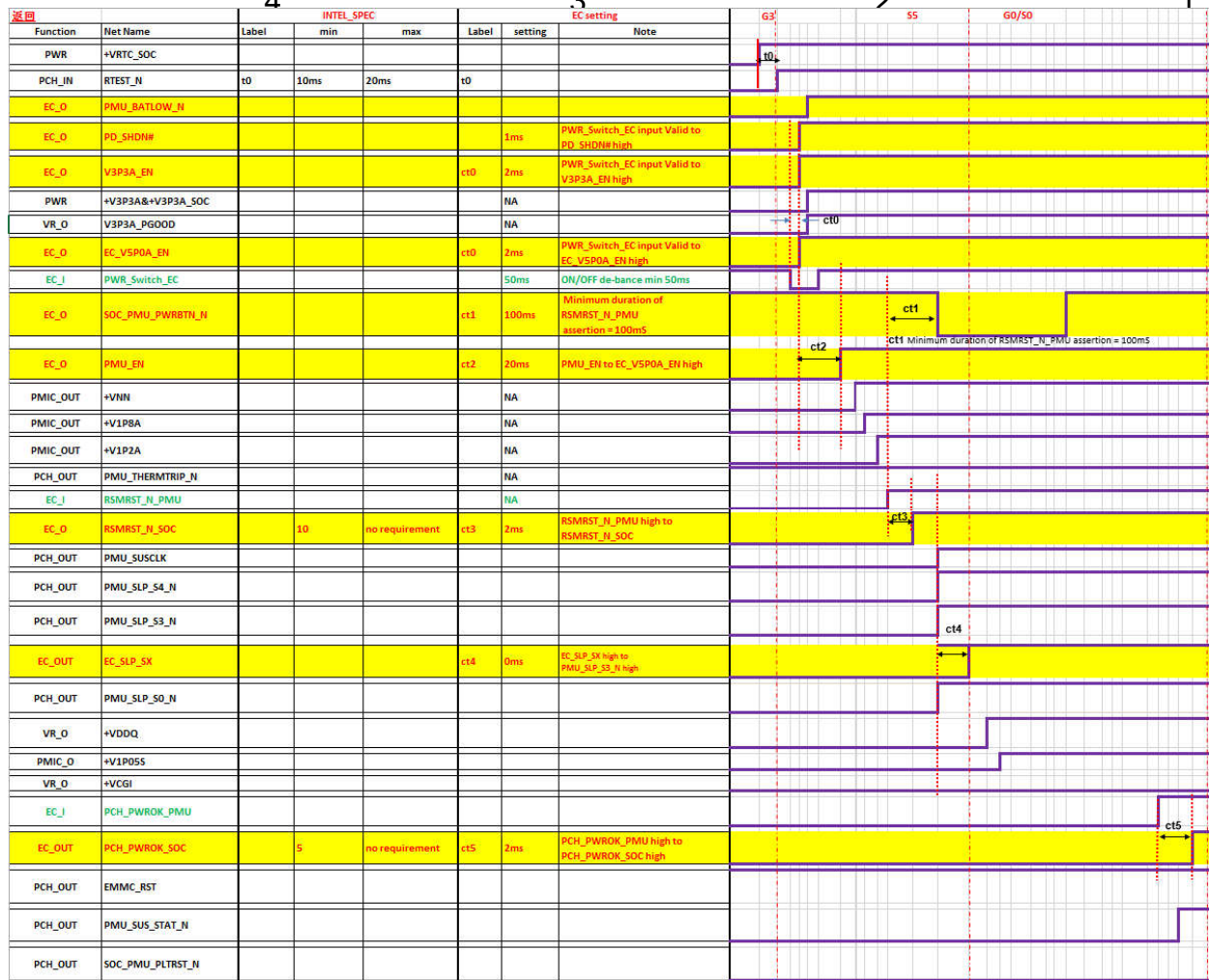
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4

3

2

1



Huaqin Telecom Technology Com.,Ltd.

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4

3

2

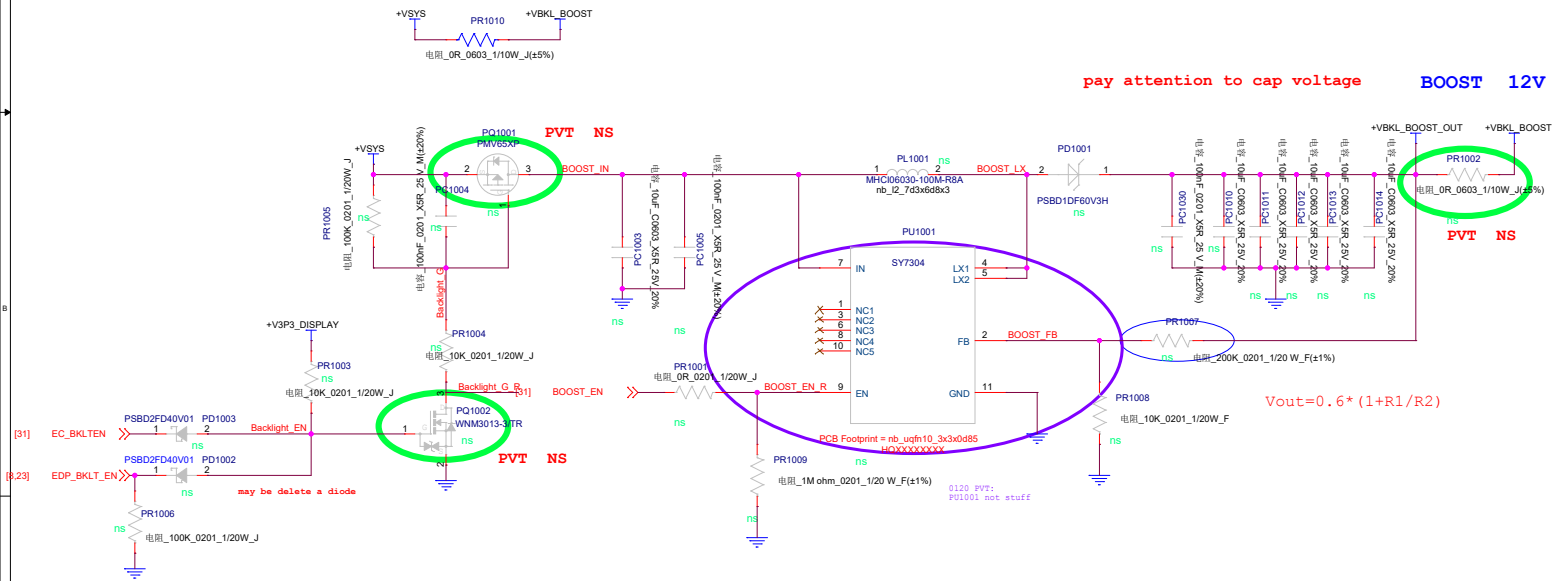
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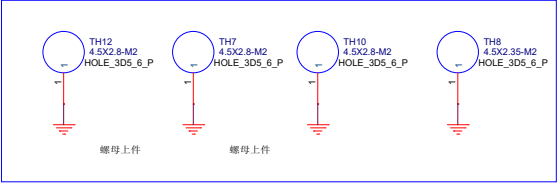
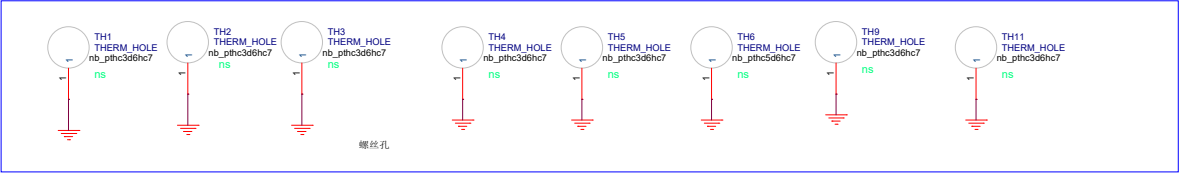
Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
LED Power Input Voltage	V _{LED}	6.0	12.0	21.0	V	1
LED Power Input Current	I _{LED}	-	TBD	TBD	mA	2
LED Power Consumption	P _{LED}	-	TBD	TBD	W	
LED Power Inrush Current	I _{LED_P}	-	-	1.5	A	3
PWM Duty Ratio		5	-	100	%	4


battery 2S need add

pay attention to cap voltage

BOOST 12V





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1.Add Battery SMBUS test point,PT603,PT604.----20180131
2.JHD01 PIN4&PIN5 NC.----20180131
3.Memory ID table order from ID0,ID1,ID2 to ID2,ID1,ID0--20180202



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